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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/761,626	01/22/2004	Meng-An Pan	2875.287000	3538

49579 7590 04/13/2009

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EXAMINER	
AGHDAM, FRESHTEH N	

ART UNIT	PAPER NUMBER
2611	

MAIL DATE	DELIVERY MODE
04/13/2009	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/761,626	PAN ET AL.	
	Examiner	Art Unit	
	FRESHTEH N. AGHDAM	2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 March 2009*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,4,6-11,14 and 16-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,4,6-11,14 and 16-26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on March 16, 2009 has been entered.

Response to Arguments

Applicant's arguments with respect to claims 1, 4, 6-11, 14, and 16-26 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 4, 7, 8, 10-14, 17, 18, and 20-25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lipka (US 7,227,910), and further in view of Doetsch et al (US 2002/0154678).

As to claims 1 and 10, Lipka discloses a method of and/ or an apparatus for modulating digital signal to higher frequency analog signal comprising: performing delta sigma modulation on a digital quadrature signal (Fig. 1, block 2); converting the modulated signal to an analog signal (block 10); converting the analog signal to an RF signal (block 12); and inherently transmitting the RF signal (via antenna 14). Lipka also teaches scrambling, pulse shaping and interpolating prior to delta sigma modulation (blocks 6-8; Col. 4, lines 59-67; Col. 5, lines 1-17). Lipka does not expressly teach adjusting a DC offset in a digital quadrature signal. One of ordinary skill in the art would recognize that it is well known and/or a matter of design choice to further include a DC offset compensation unit prior to the delta sigma modulator and after the scrambling unit of Lipka in addition to the pulse shaping (e.g. RRC) and interpolation unit as evidenced by Doestsch (Fig. 1, blocks 6-9) in order to preprocess the signal to be upconverted to an RF signal; and consequently, improving the system performance.

As to claims 4 and 14, Lipka teaches amplifying the RF signal prior to transmission (Fig. 1, block 13) in order to adjust the signal gain prior to transmission; and consequently, improving the system performance.

As to claims 7 and 17, Lipka discloses modulating the quadrature signal using one of frequency shift keying and phase shift keying (Col. 3, lines 63-67). One of ordinary skill in the art would recognize that it is obvious to use different order frequency shift keying and phase shift keying modulations based on the channel state or design requirements.

As to claims 8 and 18, Lipka discloses performing interpolation filtering on the digital quadrature signal before the delta sigma modulation (block 7).

As to claims 11, Lipka discloses a method of and/ or an apparatus for modulating digital signal to higher frequency analog signal comprising: performing delta sigma modulation on a digital quadrature signal (Fig. 1, block 2); converting the modulated signal to an analog signal (block 10); converting the analog signal to an RF signal (block 12); and inherently transmitting the RF signal (via antenna 14). Lipka also teaches scrambling, pulse shaping and interpolating prior to delta sigma modulation (blocks 6-8; Col. 4, lines 59-67; Col. 5, lines 1-17). Lipka is not explicit about using a mixer to up convert the analog signal to the RF signal. However, one of ordinary skill in the art would recognize that it is well known in the art to up utilize a mixer in order to up convert the analog signal to the RF signal to transmit the signal through the radio frequency medium. Therefore, it would have been obvious to one of ordinary skill in the art to utilize a mixer to up convert the signal to the RF signal for the reason stated above. Lipka also teaches scrambling, pulse shaping and interpolating prior to delta sigma modulation (blocks 6-8; Col. 4, lines 59-67; Col. 5, lines 1-17). Lipka does not expressly teach adjusting a DC offset in a digital quadrature signal. One of ordinary skill in the art would recognize that it is well known and/or a matter of design choice to further include a DC offset compensation unit prior to the delta sigma modulator and after the scrambling unit of Lipka in addition to the pulse shaping (e.g. RRC) and interpolation unit as evidenced by Doetsch (Fig. 1, blocks 6-9) in order to preprocess the signal to be upconverted to an RF signal; and consequently, improving the system performance.

As to claims 20-25, Lipka teaches generating the digital quadrature signal that includes an in-phase (I) component and a quadrature (Q) component (block 2), wherein the modulated signal corresponds to I and Q components that maintain substantially the same phase difference since there are not any components prior to the modulation step that changes the phase difference of 90 degrees between the I and Q components .

Claims 6, 16 and 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lipka, further in view of Hossack (US 6,819,276).

As to claims 6, 16 and 26, Lipka and Doetsch disclose all the subject matter claimed in claim 1, except for coding the modulated signal with a thermometer code. Hossack discloses a digital to analog converter that performs coding the modulated signal with a thermometer code (Fig. 3, block 120). Therefore, it would have been obvious to one of ordinary skill in the art to code the modulated signal with a thermometer code as Hossack discloses in order to reduce the number of bits that are in error.

Claims 9 and 19 arerejected under 35 U.S.C. 103(a) as being unpatentable over Lipka, further in view of Fujimori (US 6,236,912).

As to claims 9 and 19, Lipka and Doetsch disclose all the subject matter claimed in claim 8, except for the interpolation filtering reduces the digital quadrature signal from 12 bits to 10 bits. Fujimori discloses that the interpolation filtering reduces the bit width by the interpolation rate change switch within the interpolation filter (Col. 6, lines 45-52).

One of ordinary skill in the art would recognize that the exact bit width is a matter of design requirement. Therefore, it would have been obvious to one of ordinary skill in the art to output a reduced bit width signal by the interpolation filter of Lipka as taught by Fujimori in order to reduce the hardware complexity of the device/ circuitry.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to FRESHTEH N. AGHDAM whose telephone number is (571)272-6037. The examiner can normally be reached on 9:00-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chieh Fan can be reached on 571-272-3042. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/F. N. A./

Examiner, Art Unit 2611

/Chieh M Fan/

Supervisory Patent Examiner, Art Unit 2611